EAST Search History

Ref #	Hits	Search Query	DBs	Default Operator	Plurals	Time Stamp
L2	33	path same ((hdl) (vhdl) (hardware adj description adj language) (verilog)) same compil$4 and (717/123 717/13 717/143 717/144 717/155 717/156 717/137 716/3 716/5 716/16 716/18)	US-PGPUB; USPAT; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2009/04/23 16:31
L3	14	(((hdl) (vhdl) (hardware adj description adj language) (verilog)) same (register near1 transfer near1 language (rtl)) same (simulat$4 test$4) same path and net $list) and (717/123 717/138 717/143 717/144 717/155 717/156 717/137 716/3 716/5 716/16 716/18)	US-PGPUB; USPAT; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2009/04/23 16:32
L4	40	path same ((hdl) (vhdl) (hardware adj description adj language) (verilog) rtl) same compil$4 and (integrated adj circuit) and (717/123 717/13 717/143 717/144 717/155 717/156 717/137 716/3 716/5 716/16 716/18)	US-PGPUB; USPAT; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2009/04/23 16:33

L5	14	path same ((hdl) (vhdl) (hardware adj description adj language) (verilog) rtl) same compil$4 and index and (717/123 717/138 717/143 717/144 717/155 717/156 717/137 716/3 716/5 716/16 716/18)	US-PGPUB; USPAT; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2009/04/23 16:33
L6	158	((hdl) (vhdl) (hardware adj description adj language) (verilog) rtl) same compil$4 and index and (717/123 717/138 717/143 717/144 717/155 717/156 717/137 716/3 716/5 716/16 716/18)	US-PGPUB; USPAT; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2009/04/23 16:33
L7	17	((hdl) (vhdl) (hardware adj description adj language) (verilog) rtl) same compil$4 and index.clm. and (717/123 717/138 717/143 717/144 717/155 717/156 717/137 716/3 716/5 716/16 716/18)	US-PGPUB; USPAT; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2009/04/23 16:34
L8	1	((hdl) (vhdl) (hardware adj description adj language) (verilog) rtl) same compil$4 and index.clm. and (717/123 717/138 717/143 717/144 717/155 717/156 717/137 716/3 716/5 716/16 716/18)	US-PGPUB	OR	ON	2009/04/23 16:34

L9	11	(net$list) same ((hdl) (vhdl) (hardware adj description adj language) (verilog)) same path and (717/123 717/138 717/139 717/13/ 717/143 717/144717/155 717/156 717/137 716/3 716/5 716/16 716/18)	US-PGPUB	OR	ON	2009/04/23 16:34
L11	3	(generat$4 construct$4 creat$4 build$4) with ((hardware adj description adj language) (hdl)) same pars$4 with (description file) same path and (717/123 717/138 717/139 717/138 717/143 717/144 717/155 717/156 717/137 716/3 716/5 716/16 716/18)	US-PGPUB; USPAT; USOCR; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2009/04/23 16:37
L12	11	(net$list) same ((hdl) (vhdl) (hardware adj description adj language) (verilog)) same path and (717/123 717/138 717/139 717/13 717/143 717/144 717/155 717/156 717/137 716/3 716/5 716/16 716/18)	US-PGPUB	OR	ON	2009/04/23 16:38
L13	94	(((hdl) (vhdl) (hardware adj description adj language) (verilog) asci) same (register near1 transfer near1 language (rtl)) same (simulat$4 test$4) same (Ic near2 design) and net$list (file adj path)) and (717/101 717/123 717/138 717/143 717/144 717/155 717/156 717/137 716/3 716/5 716/16 716/18)	US-PGPUB; USPAT; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2009/04/23 16:56

L15	15	(((hdl) (vhdl) (hardware adj description adj language) (verilog) asci) same (register near1 transfer near1 language (rtl)) same (simulat$4 test$4) same (lc near2 design) and net$list (file adj path) and (rapid $make)) and (717/101 717/123 717/138 717/143 717/144 717/155 717/156 717/137 716/3 716/5 716/16 716/18)	US-PGPUB; USPAT; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2009/04/23 16:56
L16	1	(((hdl) (vhdl) (hardware adj description adj language) (verilog) asci) same (register near1 transfer near1 language (rtl)) same (simulat$4 test$4) same (lc near2 design) and net$list (file adj path) and (rapid $make)) and (717/101 717/123 717/138 717/143 717/144 717/138 717/155 717/156 717/137 716/3 716/5 716/16 716/18)	US-PGPUB	OR	ON	2009/04/23 16:57
L17	9	(((hdl) (vhdl) (hardware adj description adj language) (verilog) asci) same (register near1 transfer near1 language (rtl)) same (simulat$4 test$4) same (lc near2 design) and net$list (file adj path)).clm. and (717/101 717/123 717/138 717/143 717/144 717/155 717/156 717/137 716/3 716/5 716/16 716/18)	US-PGPUB; USPAT; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2009/04/23 16:57

L18	40	path same ((hdl) (vhdl) (hardware adj description adj language) (verilog) rtl) same compil$4 and (integrated adj circuit) and (717/123 717/13/ 717/143 717/144 717/155 717/156 717/137 716/3 716/5 716/16 716/18)	US-PGPUB; USPAT; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2009/04/23 16:57
L19	6	path same ((hdl) (vhdl) (hardware adj description adj language) (verilog) rtl) same compil$4 same (integrated adj circuit) and (717/123 717/13/ 717/143 717/144 717/155 717/156 717/137 716/3 716/5 716/16 716/18)	US-PGPUB; USPAT; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2009/04/23 16:58
L20	15	(((hdl) (vhdl) (hardware adj description adj language) (verilog) asci) same (register near1 transfer near1 language (rtl)) same (simulat$4 test$4) same (lc near2 design) and net$list (file adj path) and (rapid $make)) and (717/101 717/123 717/138 717/143 717/144 717/155 717/156 717/137 716/3 716/5 716/16 716/18)	US-PGPUB; USPAT; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2009/04/23 17:02
L21	15	(((hdl) (vhdl) (hardware adj description adj language) (verilog) asci) same (register near1 transfer near1 language (rtl)) same (simulat$4 test$4) same (lc near2 design) and net$list (path) and (rapid$make)) and (717/101 717/123 717/138 717/143 717/144 717/155	US-PGPUB; USPAT; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2009/04/23 17:05

		717/156 717/137 716/3 716/5 716/16 716/18)				
L24	3	(((hdl) (vhdl) (hardware adj description adj language) (verilog) asci) same (lc near2 design) and net$list (path) and (rapid $make)).clm. and (717/101 717/123 717/138 717/143 717/144 717/155 717/156 717/137 716/3 716/5 716/16 716/18)	US-PGPUB; USPAT; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2009/04/23 17:05
S31	7	(pars$4 analyz44) with (description) same ((hdl) (vhdl) (hardware adj description adj language)) same path	US-PGPUB; USPAT; USOCR; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2009/04/20 13:08
S34	19	(pars$4 analyz44) with (description) same ((hdl) (vhdl) (hardware adj description adj language)).clm.	US-PGPUB; USPAT; USOCR; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2009/04/20 13:11
S35	8	(pars$4 analyz44) with (description) same ((hdl) (vhdl) (hardware adj description adj language)).clm.	US-PGPUB	OR	ON	2009/04/20 13:11
S63	9	(((hdl) (vhdl) (hardware adj description adj language) (verilog) asci) same (register near1 transfer near1 language (rtl)) same (simulat$4 test$4) same (lc near2 design) and net$list (file adj path)).clm. and (717/101 717/123 717/138 717/143 717/144717/155 717/156 717/137 716/3 716/5 716/16 716/18)	US-PGPUB; USPAT; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2009/04/20 13:56

S64	33	path same ((hdl) (vhdl) (hardware adj description adj language) (verilog)) same compil$4 and (717/123 717/13/ 717/143 717/144717/155 717/156 717/137 716/3 716/5 716/16 716/18)	US-PGPUB; USPAT; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2009/04/20 14:36
S65	51	path same ((hdl) (vhdl) (hardware adj description adj language) (verilog) rtl) same compil$4 and (717/123 717/13/ 717/143 717/144717/155 717/156 717/137 716/3 716/5 716/16 716/18)	US-PGPUB; USPAT; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2009/04/20 14:36

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